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Attorney Docket No: NVID001/00US

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of Priem *et al.*

Serial No.: 09/056,656 Examiner: U. Chauhan

Filed: April 7, 1998 Art Unit: 2671

For: **TEXTURE CACHE FOR A COMPUTER GRAPHICS ACCELERATOR**

BOX AF
Assistant Commissioner for Patents
Washington, D.C. 20231

RESPONSE

Responsive to the Final Official Action of November 29, 2001, the due date being extended three months to May 29, 2002, Applicants respectfully request reconsideration of the above-identified application in view of the following remarks.

Rejections under 35 U.S.C. §103

At paragraphs 4-6 of the Office Action, the Examiner rejected claims 42-44, 52-54, 70-73, 81, 90, 91, and 99 as being unpatentable over U.S. Patent No. 5,987,567 to Rivard et al. ("Rivard") and U.S. Patent No. 6,259,460 to Gossett et al. ("Gossett").

At paragraphs 7-12 of the Office Action, the Examiner rejected claims 45, 46, 48, 49, 51, 55, 56, 58, 59, 61, 74, 75, 77, 78, 80, 92, 93, 94, 96, and 98 as being unpatentable over Rivard, Gossett and U.S. Patent No. 5,790,130 to Gannett ("Gannett").

At paragraphs 13-14, the Examiner rejected claims 47, 57, 76, and 94 as being unpatentable over Rivard, Gossett and U.S. Patent No. 5,926,187 to Kim.

Based on the attached Declaration Under 37 CFR 1.131 by Curtis Priem, Gopal Solanki, and David Kirk in Support of Antedating Reference ("Declaration") and the supporting Exhibits, Applicants submit that they have established an invention date prior to the effective date of Gossett of the inventions claimed in claims 42, 43, 47-49, 51-53, 57-59, 61, 70-72, 76-78, 80, 81, 90, 94-96, 98, and 99. The rejections of claims 42, 43, 47-49, 51-53, 57-59, 61, 70-72, 76-78, 80, 81, 90, 94-96, 98, and 99 are therefore traversed.

As set forth in the Declaration, the inventions claimed in claim 42, 70, and 71 were actually reduced to practice before the March 26, 1998 effective date of Gossett ("the Critical Date"). This actual reduction to practice was embodied in NVIDIA's RIVA 128 product, which was described in NVIDIA's Graphics Reference Manual before the Critical Date, publicly launched before the Critical Date and shipped to customers before the Critical Date. *See* paragraphs 1-6 of the Declaration. The RIVA 128 product included a texture cache memory that stores texel data to be used by a graphic engine to produce texture values for pixels, a cache controller that performs a replacement policy determination for texel data to be stored in the texture cache memory, and a direct memory access (DMA) engine that retrieves texel data from memory. *See* paragraphs 7-9 of the Declaration. The RIVA 128 product was used before the Critical Date in a graphics accelerator that operated in a system including a central processing unit (CPU), memory, and a system bus. *See* paragraph 13 of the Declaration. Thus, the

inventions of claim 42, 70, and 71 were actually reduced to practice before the Critical Date.

As set forth in paragraph 14 of the Declaration, the RIVA 128 product was used before the Critical Date in a process to retrieve texel data from memory via a direct memory access engine, store retrieved texel data in a texture cache memory based on a replacement policy determination performed by a cache controller, and render a polygon using texel data stored in the texture cache memory. Thus, the invention of claim 52 was actually reduced to practice before the Critical Date.

As set forth in paragraph 10 of the Declaration, the texture cache memory of the RIVA 128 product was fully associative. Thus, the inventions of claims 43, 53, 72, and 90 were actually reduced to practice before the Critical Date.

As set forth in paragraph 11 of the Declaration, the RIVA 128 product implemented virtual-physical address translation. Thus, the inventions of claims 47, 57, 76, and 94 were actually reduced to practice before the Critical Date.

As set forth in paragraph 12 of the Declaration, the RIVA 128 product included support for a prefetch mode and a non-prefetch mode. Thus, the inventions of claims 48, 49, 58, 59, 77, 78, 95, and 96 were actually reduced to practice before the Critical Date.

As set forth in paragraph 13 of the Declaration, the RIVA 128 product was included in a graphics accelerator board prior to the Critical Date. Thus, the inventions of claims 81 and 99 were actually reduced to practice before the Critical Date.

As noted above, claims 44, 54, 73, and 91 were rejected as being unpatentable over Rivard and Gossett. Even if Rivard and Gossett teach what the Examiner alleges, the Examiner has not presented a *prima facie* case of obviousness. Claims 44, 54, 73,

and 91 recite a replacement policy determination that is performed in accordance with a least recently loaded policy. *See, e.g.*, page 20 of Applicants' specification. What the Examiner appears to allege, on the other hand, is a least recently used policy. For at least this reason, the rejection of claims 44, 54, 73, and 91 is traversed.

As noted above, claims 45, 55, 74, and 92 were rejected as being unpatentable over Rivard, Gossett and Gannett. Even if Rivard, Gossett, and Gannett teach what the Examiner alleges, the Examiner has not presented a *prima facie* case of obviousness. Claims 45, 55, 74, and 92 recite a replacement policy determination such that cache lines containing texels that are being used to compute texture values to describe a polygon cannot be overwritten until the polygon is complete. *See, e.g.*, page 19 of Applicants' specification. What the Examiner appears to allege, on the other hand, is a replacement policy that is based on the history of usage a texture block and the priority of the textures stored in the blocks. *See*, col. 10, lines 59-64 of Gannett. While priorities can be based on various user-defined and internal-default considerations, the replacement policy of Gannett seems to be confined to independent considerations of individual texture blocks. This policy is in contrast to Applicants' policy that can consider a common priority scheme for a plurality of cache lines. For at least this reason, the rejection of claims 45, 55, 74, and 92 is traversed.

Claims 46, 56, 75, and 93 are dependent on claims 45, 55, 74, and 92, respectively. Accordingly, the rejection of claims 46, 56, 75, and 93 is traversed for at least the reasons stated above with respect to claims 45, 55, 74, and 92.

Finally, Applicants note that the swearing back of Gossett alone does not constitute an admission by the Applicants that the other cited references are prior art

against Applicants' invention. Applicants reserve the right to submit further evidence to antedate one or more of the other cited references. Applicants also reserve the right to antedate one or more of the cited references with respect to the rejections of claims 44-46, 54-56, 73-75, and 91-93.

Conclusion

All of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding rejections, and that they be withdrawn. The Examiner is invited to telephone the undersigned representative if an interview might be useful for any reason.

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Respectfully submitted,
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